

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A silicon carbide semiconductor device, comprising:  
a first deposition film (2) of low concentration silicon carbide of a first conductivity type formed on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;  
a second deposition film (31) formed on the first deposition film (2) comprising a high concentration gate region of a second conductivity type having a selectively removed first region;  
a third deposition film (32) formed on the second deposition film (31) comprising a second region that is wider than the selectively removed first region, a high concentration source region (5) of a first conductivity type and a low concentration gate region of a second conductivity type;  
a low concentration base region (4) of a first conductivity type formed in contact with the first deposition film (2) in the first and second regions;  
a gate insulation film (6) formed on at least a surface of the third deposition film (32);  
a gate electrode (7) formed via the gate insulation film (6);  
a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate of a first conductivity type; and  
a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (32) of a second conductivity type.

Claim 2 (Currently Amended): A silicon carbide semiconductor device according to claim 1, wherein the third deposition film (32) has a thickness within a range of 0.2  $\mu\text{m}$  to 0.7

$\mu\text{m}$  and wherein the low concentration gate region (11) of a second conductivity type selectively formed in the third deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration higher than  $1 \times 10^{15} \text{ cm}^{-3}$  and lower than  $5 \times 10^{15} \text{ cm}^{-3}$ .

**Claim 3 (Currently Amended):** A silicon carbide semiconductor device according to claim 1 or 2, wherein the low concentration base region (4) of a first conductivity type has an upper surface having at least a portion thereof in contact with the gate insulation film (6) and provided therein with a cavity (41).

**Claim 4 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 3~~ claim 1, wherein the low concentration base region (4) of a first conductivity type has a lower impurity concentration than the high concentration gate region (31) of a second conductivity type.

**Claim 5 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 4~~ claim 1, wherein the low concentration gate region (11) of a second conductivity type selectively formed in the third deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration of not higher than  $2 \times 10^{16} \text{ cm}^{-3}$ .

**Claim 6 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 5~~ claim 1, wherein the low concentration base region (4) of a first conductivity type selectively formed in the third deposition film (32) has a portion that is in

contact with the high concentration gate region (31) of a second conductivity type and has an impurity concentration of not higher than  $4 \times 10^{16} \text{ cm}^{-3}$ .

**Claim 7 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 6~~ claim 1, wherein the high concentration gate region (31) of a second conductivity type is the second deposition film (31) of silicon carbide formed on the first deposition film-(2).

**Claim 8 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 7~~ claim 1, wherein the gate insulation film (6)-formed on the third deposition film has at least a portion thicker than other portions on the low concentration base region (4) of a first conductivity type selectively formed in the third deposition film-(32).

**Claim 9 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 8~~ claim 1, wherein above a surface of the base region (4) of a first conductivity type selectively formed in the third deposition film-(32), the gate electrode (7) has at least a portion removed.

**Claim 10 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 9~~ claim 1, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (11-20) plane.

**Claim 11 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 1 to 10~~ claim 1, wherein in terms of crystal Miller index the surface of the

silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (000-1) plane.

Claim 12 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 1 to 11~~ claim 1, wherein the low concentration gate region (11) of a second conductivity type has a portion that is in contact with the gate insulation film (6) and has a buried channel region (91) of a first conductivity type.

Claim 13 (Currently Amended): A silicon carbide semiconductor device, comprising:

a lower deposition film (2) of low concentration silicon carbide of a first conductivity type formed on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;

a high concentration gate region (31) of a second conductivity type selectively formed in the lower deposition film (2) so that a first region of low concentration silicon carbide of a first conductivity type remains in the lower deposition film;

an upper deposition film (32) on the lower deposition film (2), comprising a low concentration base region (4) of a first conductivity type that is a second region wider than the first region, a high concentration source region (5) of a first conductivity type and a low concentration gate region (11) of a second conductivity type;

a gate insulation film (6) formed on at least a surface of the upper deposition film (32);

a gate electrode (7) formed via the gate insulation film (6);

a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate (1) of a first conductivity type; and

a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

**Claim 14 (Currently Amended):** A silicon carbide semiconductor device according to claim 13, wherein the upper deposition film (32) has a thickness within a range of 0.2  $\mu\text{m}$  to 0.7  $\mu\text{m}$  and wherein the low concentration gate region (11) of a second conductivity type selectively formed in the upper deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration higher than  $1 \times 10^{15} \text{ cm}^{-3}$  and lower than  $5 \times 10^{15} \text{ cm}^{-3}$ .

**Claim 15 (Currently Amended):** A silicon carbide semiconductor device according to claim 13-~~or~~-14, wherein the low concentration base region (4) of a first conductivity type has a lower impurity concentration than the high concentration gate region (51) of a second conductivity type.

**Claim 16 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 13 to 15~~ claim 13, wherein the low concentration gate region (11) of a second conductivity type selectively formed in the upper deposition film (32) has a portion that is in contact with the gate insulation film (6) and has an impurity concentration of not higher than  $2 \times 10^{16} \text{ cm}^{-3}$ .

**Claim 17 (Currently Amended):** A silicon carbide semiconductor device according to ~~any of claims 13 to 16~~ claim 13, wherein the upper deposition film (32) is constituted of silicon carbide.

Claim 18 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 13 to 17~~ claim 13, wherein the gate insulation film (6) formed on the upper deposition film (32) has at least a portion that is thicker than other portions on the low concentration base region (4) of a first conductivity type selectively formed in the upper deposition film (32).

Claim 19 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 13 to 18~~ claim 13, wherein on the surface of the base region (4) of a first conductivity type selectively formed in the upper deposition film (32), the gate electrode (7) has at least a portion removed.

Claim 20 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 13 to 19~~ claim 13, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (11-20) plane.

Claim 21 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 13 to 20~~ claim 13, wherein in terms of crystal Miller index the surface of the silicon carbide substrate (1) of a first conductivity type is a plane that is parallel to a (000-1) plane.

Claim 22 (Currently Amended): A silicon carbide semiconductor device according to ~~any of claims 13 to 21~~ claim 13, wherein the low concentration gate region (11) of a

second conductivity type has a portion that is in contact with the gate insulation film (6) and has a buried channel region (91) of a first conductivity type.

Claim 23 (Currently Amended): A method of manufacturing a silicon carbide semiconductor device, comprising ~~at least the steps of:~~

forming a first deposition film (2) of low concentration silicon carbide of a first conductivity type on a surface of a high concentration silicon carbide substrate (1) of a first conductivity type;

forming on the first deposition film (2) a second deposition film (31) having a first region from which a high concentration region of a second conductivity type has been selectively removed;

forming on the second deposition film (31) and on the selectively removed first region a third deposition film (32) comprised of a low concentration region of a second conductivity type;

selectively forming a second region in the third deposition film (32) that is wider than the first region by forming a low concentration base region (4) of a first conductivity type in the first and second regions in contact with the first deposition film (2) of low concentration silicon carbide of a first conductivity type, and selectively forming a source region (5) constituted of a high concentration of silicon carbide of a first conductivity type in the third deposition film (32);

forming a gate insulation film (6) on at least the surface of the third deposition film (32);

forming a gate electrode (7) via the gate insulation film (6);

forming a drain electrode (10) having a low-resistance contact connection on a backside of the silicon carbide substrate (1) of a first conductivity type; and

forming a source electrode (8) having a low-resistance contact connection with part of the high concentration source region (9) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

Claim 24 (Currently Amended): A method of manufacturing a silicon carbide semiconductor device according to claim 23, further comprising the steps of:

forming the second deposition film (31) on the first deposition film (2);

forming a trench (41) that extends from the surface of the second deposition film (31) to the first deposition film (2);

forming the third deposition film (32) on the second deposition film (31) and the trench (41); and

selectively implanting impurity ions of a first conductivity type to form the low concentration base region (4) of a first conductivity type in the third deposition film (32).

Claim 25 (Currently Amended): A method of manufacturing a silicon carbide semiconductor device, comprising ~~at least the steps of:~~

forming a lower deposition film (2) of low concentration silicon carbide of a first conductivity type on a surface of a silicon carbide substrate (1) of a first conductivity type;

forming an impurity region (31) of a second conductivity type in the lower deposition film (2);

forming an upper deposition film (32) constituting a low concentration gate region (11) of a second conductivity type on the lower deposition film (2) in which the impurity region (31) of a second conductivity type is formed;

forming a high concentration source region (5) of a first conductivity type on the upper deposition film (32);

forming in the upper deposition film (32) a low concentration base region (4) of a first conductivity type in contact with the lower deposition film (2);

forming a gate insulation film (6) on at least a surface of the upper deposition film (32);

forming a gate electrode (7) via the gate insulation film (6);

forming a drain electrode (10) having a low-resistance contact connection with a backside of the silicon carbide substrate (1) of a first conductivity type; and

forming a source electrode (9) having a low-resistance contact connection with part of the high concentration source region (5) of a first conductivity type and the low concentration gate region (11) of a second conductivity type.

Claim 26 (Currently Amended): A method of manufacturing a silicon carbide semiconductor device according to claim 25, further comprising the steps of:

forming the impurity region of a second conductivity type in the lower deposition film (2) of low concentration silicon carbide by implantation of a high concentration of impurity ions of a second conductivity type, and forming the upper deposition film (32) thereon; and

selectively implanting impurity ions of a first conductivity type in the upper deposition film (32) to form the low concentration base region (4) of a first conductivity type.